

Latches and Flip-Flops

Gate ICs used: 7476, 7474, 7400

7.0 Introduction:

In this lab you will investigate several types of flip flops and see how they are used in various applications and how they can be controlled.

7.1 The basic flip-flop: cross coupled NANDs and NORs

Figure 7.1 shows the basic circuits for a simple flip flop using two NAND gates, of which the outputs of each are connected to the inputs of the other. Also shown is a model which can be used to analyze the behavior of this simple circuit.

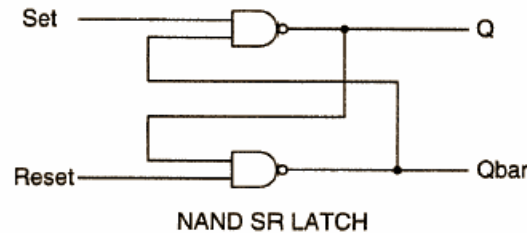


Figure 7.1 NAND SR Latch

Task 1

Using a 7400 construct the circuit in figure 7.1 and verify its operation. Use two switches for the control inputs (SET and RESET) and monitor both latch output (Q and Qbar), construct truth table and answer the following questions:

1. How do you set the latch? What is the condition of the latch's two outputs (Q and Qbar) when the latch is set?
2. How do you reset the latch? What is the condition of the latch's output when the latch is reset?
3. What happens to a NAND latch in the invalid state?
4. Are the latch control inputs active-high or active-low?

7.2 Clocked D and J-K flip flop:

Figure 7.2(a) shows the schematic symbols of edge-triggered JK and D flip flop. The term edge-triggered refers to the fact the outputs change only on active edge of the clock: low to high for 7474, D flip flop, and high to low for 7476, the JK flip flop. Thus for the D FF, the output Q will take whatever value D has when the clock goes from a low to high.

Each of the flip flops shown in figure 7.2 have asynchronous set, SET, and reset, CLR, lines. These signals are used to set or reset the flip flop regardless of any activity on the other inputs. Thus the term "asynchronous" means the flip flops can be controlled with out the use of the clock signal

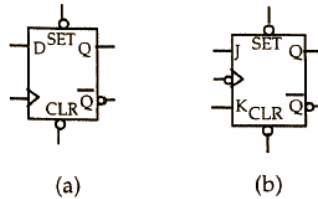


Figure 7.2 Edge-triggered D (a), and JK (b) flip flop

Task 2: Test the operation of JK(7476 FF) and D (7474 FF)

Leave the J, K, D and clock inputs unconnected and verify that the asynchronous inputs SET, CLR, cause the outputs to change accordingly. Connect the flip-flops J, K, SET and CLR control inputs to switches, the clock to a pulse generator, and the outputs to LEDs. Construct truth table and answer the following questions on JK FF:

1. Which control inputs are asynchronous? Which control inputs are synchronous?
2. Determine how to asynchronously store a 0 or a 1 in the flip-flop?
3. Which control inputs (synchronous versus asynchronous) have a priority?

Attention:

You need to turn in Lab report for this project (one per group); here is the lab report format:

Report Format

First Page:

EET 2141

Lab #

Group Members

Comments about this Lab

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