

EET 2141 - DIGITAL SYSTEMS/MICROPROCESSORS BASICS
4 CREDITS - (3 Hours Recitation + 2 Hours Lab)
Fall 2009

Course Description: Introduction to digital logic circuits. Number systems, codes, Boolean algebra, logic gates, combinational logic, sequential logic circuits.

Instructor: Dr. Nasser Alaraje
Phone: 487-1661
Office: EERC 417
E-mail: alaraje@mtu.edu

Office Hours: MWF 3:00 – 5:00 pm (or by appointment)

Prerequisite: EET1120 or EET1411 or EET2311

Classroom/Time: MWF 2:05 – 2:55 pm, EERC 315

Lab/Time: T 11:05 am– 12:55 pm, EERC 427

Course Webpage: <http://www.tech.mtu.edu/~alaraje/Fall2009/EET2141/EET2141Fall2009.html>

Text Book: Digital Systems: Principles and Applications by R. J. Tocci and N. S. Widmer, the 10th edition, Prentice Hall, 2007

References: 1. Digital Design Fundamentals (2nd ed.), K. J. Breeding, Simon & Schuster, 1992.

Goals: To become familiar with the combinational switching theory, Boolean algebra, and clocked sequential networks.

Objectives: Students should be able to:

1. Understand the basic logic gates and combinational logic functions, symbols, truth tables, timing diagrams, and logic circuits.
2. Simplify complex logic circuits by applying Boolean algebra laws and theorems and Karnaugh mapping.
3. Understand the operation of basic counters, decoders, multiplexers and arithmetic circuits.
4. Convert between the decimal, binary, hexadecimal, and octal number systems.
5. Understand binary, and BCD, the parity method for error detection, and the need for alphanumeric codes, especially the ASCII code.
6. Perform binary addition, subtraction, multiplication, and division on binary (using the 2's-complement system) and hexadecimal numbers.
7. Understand the basic types of flip-flop.
8. Understand sequential logic systems including synchronous and asynchronous operation.
9. Use modern computer tools for digital design/verification using VHDL.
10. understand the characteristics of modern programmable logic devices

Topics:

1. Binary codes and Arithmetic
2. Boolean and Switching algebras
3. Gates; physical implementation
4. Combinational logic design techniques
5. Sequential circuits: analysis and design
6. Introduction to programmable logic devices
7. Digital design using VHDL

Grading:

Your final grade is based on the grade weighting plan below which gives you the highest grade, 75% of your grade toward class as follows:

	<u>Plan A</u>	<u>Plan B</u>	
Homework, quizzes, computer projects	20%	20%	
Hour exams	60%	20%	Week 5 and Week 10
Final exam	20%	60%	

Your lab assignments represents 25% of your total grade

Scale:

90-100	A	70-74	C
85-89	AB	65-69	CD
80-84	B	60-64	D
75-79	BC	0 -59	F

Computer Usage:

Xilinx webpack contains v. 7.1i, Mentor Graphics ModelSim software v.6.1

Cheating:

University rules require that any student caught cheating or copying from another student receive a failing grade for the course and be reported to the Dean of Students. **Copying includes copying or sharing any part of a computer file.**

Copying Software:

Most software packages are copyrighted and protected under the laws of the United States. Anyone who copies such a software package in violation of the software license is committing a Federal offense and is subject to prosecution.

Make-up policy:

- The final examination may only be taken at the scheduled time. You *must not* make travel plans that conflict with the final exam schedule.
- Midterm examinations may be made up only due to illness on the day of the exam (a doctor's note is required) or by advance arrangement (a written request one week in advance of the exam is required). The instructor reserves the right to deny any advance request for a make-up exam.

Use of Electronic Devices:

Cell phones, Blackberries, iPods, PDAs, or any other electronic devices **are not to be used in the classroom.** Please make sure to bring a calculator with you to class. Calculators on other devices are strictly prohibited. Information exchanges on these devices during class are also prohibited and violate the Academic Integrity Code of Michigan Tech.

University Policies:

Academic regulations and procedures are governed by University policy. Academic dishonesty cases will be handled in accordance the University's policies. If you have a disability that could affect your performance in this class or that requires an accommodation under the Americans with Disabilities Act, please see me as soon as possible so that we can make appropriate arrangements. The Affirmative Action Office has asked that you be made aware of the following:

Michigan Tech complies with all federal and state laws and regulations regarding discrimination, including the Americans with Disabilities Act of 1990. If you have a disability and need a reasonable accommodation for equal access to education or services at Michigan Tech, please call the Dean of Students Office, at 487-2212. For other concerns about discrimination, you may contact your advisor, department head or the Affirmative Action Office, at 487-3310

Academic Integrity: http://www.studentaffairs.mtu.edu/dean/judicial/policies/academic_integrity.html

Affirmative Action: <http://www.admin.mtu.edu/aao/>

Disability Services: http://www.admin.mtu.edu/urel/studenthandbook/student_services.html#disability

Changes:

This syllabus is subject to change as found appropriated by the instructor. The changes will be announced in class in a timely fashion.